CLAIMS

What is claimed is:

1. A clock and data recovery circuit comprising:

a clock signal generator for generating a plurality of clock signals, each clock signal having a different phase with respect to the others;

a phase selector for selecting one of the clock signals of the plurality of clock signals as a recovered clock signal if a first of the plurality of clock signals is in a first state and if a second of the plurality of clock signals is in a second state when a logic level transition of a received data is detected,

a recovered data generator for generating a recovered data that is synchronized with the recovered clock signal output from the phase selector, using the received data.

2. The clock and data recovery circuit of claim 1 wherein the clock signals have a phase difference of 360/N x K from each other, wherein N denotes an integer and wherein K denotes an integer from 0 to N-1.

3. The clock and data recovery circuit of claim 2 wherein the phase selector generates an $I+2_{th}$ clock signal out of the N clock signals as the recovered clock signal, wherein the first of the plurality of clock signals is

an I_{th} clock signal and wherein the second of the plurality of clock signals is an $I+1_{th}$ clock signal, wherein I denotes an integer from 1 to N.

4. The clock and data recovery circuit according to claim 3, wherein the phase selector comprises:

N flip-flops for receiving the N clock signals and generating N clock signals and N complementary clock signals when a level transition of the received data is detected;

N AND gates for performing AND operation of an I_{th} complementary clock signal and an $I+1_{th}$ clock signal out of the N clock signals and the N complementary clock signals; and

N switches for generating the $I+2_{th}$ clock signal as the recovered clock signal in response to corresponding output signals of the N AND gates.

5. The clock and data recovery circuit according to claim 4, wherein the recovered data generator receives the received data and generates the recovered data in response to the complementary signal of the recovered clock signal.

6. A method for recovering clock and data information from a signal comprising:

generating a plurality of clock signals, each clock signal having a different phase with respect to the others;

selecting one of the clock signals of the plurality of clock signals as a recovered clock signal if a first of the plurality of clock signals is in a first state and if a second of the plurality of clock signals is in a second state when a logic level transition of a received data is detected,

generating a recovered data that is synchronized with the recovered clock signal output from the phase selector, using the received data.

7. The method of claim 6 wherein the clock signals have a phase difference of 360/N x K from each other, wherein N denotes an integer and wherein K denotes an integer from 0 to N-1.

8. The method of claim 7 wherein an $I+2_{th}$ clock signal out of the N clock signals is generated as the recovered clock signal, wherein the first of the plurality of clock signals is an I_{th} clock signal and wherein the second of the plurality of clock signals is an $I+1_{th}$ clock signal, wherein I denotes an integer from 1 to N.

9. The method according to claim 8, wherein the step of generating the recovered clock signal comprises steps of:

generating N clock signals and N complementary clock signals by receiving the N clock signals when a level transition of the received data is detected;

generating N AND operation signals by performing an AND operation of an I_{th} complementary clock signal and an $I+1_{th}$ clock signal out of the N clock signals and the N complementary clock signals; and

generating an $I+2_{th}$ clock signal as the recovered clock signal in response to the N AND operation signals.

10. The method according to claim 9, wherein the step of generating the recovered data generates the recovered data by using the received data in response to a complementary signal of the recovered clock signal.